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02/19/02

U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10079472	02/19/2002	257		2314	
APPLICANTS: Mahajan, Maitreyee; Walker, Andrew; Kouznetsov, Igor,					
**CONTINUING DATA VERIFIED: <i>NC</i>					
FOREIGN APPLICATIONS VERIFIED: <i>NC</i>					
PG-PUB DO NOT PUBLISH <input type="checkbox"/> RESCIND <input type="checkbox"/>					
Foreign priority claim <input type="checkbox"/> yes <input checked="" type="checkbox"/> no				ATTORNEY DCKET NO	
35 USC 119 condition met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no				40025-005	
Verified and Acknowledged Examiner's initials					
TITLE : Gate dielectric structures for integrated circuits and methods for making and using such gate dielectric structures					
U.S. DEPT. OF COMM./PAT. & TM.-PTO: 136L (Rev. 12-95)					

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NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
ISSUE FEE		Sheets Drwg.	Figs. Drwg.
Amount Due	Date Paid	Print Fig.	
Primary Examiner		Application Examiner	
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	
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